## Digital Front-end Transition card

This card receives four 28 bit wide busses from the DFE mother board via the backplane connectors that the two are plugged into. Two of the busses (top and bottom muon) are buffered; each of these busses flow to: a G-link connector (20 bits), an AMCC link connector (16 bits) and also to a 28 bit LVDS transmitter chip (28 bits). This gives the user the option of three different outputs for each of these busses. The other two busses (top and bottom L1L2) connect directly to two parallel LVDS transmitter chips. All of the LVDS outputs are wired to an Amp 2mm hard metric cable to board connector. This connector requires special 2mm HM cable assemblies made by Amp (and a couple other companies) using shielded, flat, twin cable with a differential impedance of 100 ohms.

The reset from the DFE mother board is buffered and wired to the two G-link connectors. The clock signal is conditioned with a special 10 output clock buffer. This provides a separate clock signal for each of the 10 destinations: two G-links, two AMCC links and six LVDS chips.

The chips used: 74LCX16244 (Fairchild 16 bit buffer), P16C2510A (Pericom 10 output clock buffer), SN65LVDS93 (Texas Instruments LVDS serializer/deserializer transmiter).

Major parts count:			
Item	Quantity	Part	Number
A	1	Type A 2mm HM	Amp # 352068-1
В	1	Type B 2mm HM	Amp # 352069-1
C	1	Type C 2mm HM	Amp # 352115-1
D	4	74LCX16244MTD	48-lead (TSSOP) package
E	1	P16C2510AL	24-lead (TSSOP) package
F	6	SN65LVDS93DGG	56-lead (TSSOP) package
G	2	PCB connector (G-link)	Amp #104078-6
Н	2	PCB connector (AMCC)	Samtec #SFM115-02-SDLC
I	1	Type B 2mm HM	Amp # 1-106014-1
J	4	2mm header	Molex #87089-2816

